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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,492	04/21/2004	Sadami Takeoka	60188-820	5291

7590 10/23/2006
McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/828,492

Applicant(s)

TAKEOKA ET AL.

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-18 is/are pending in the application.
- 4a) Of the above claim(s) 17 and 18 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14 and 15 is/are allowed.
- 6) ☒ Claim(s) 11-13 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/187,269.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The amendment filed on 09/07/2006 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11,12,13, and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The "internal combinational circuit provided in each of said chip IPs," recited at line 7 of claim 11, is not part of applicant's original disclosure.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 11,12,13, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "combinational circuit" in claim 11 is used by the claim to mean (consistent with applicant's original disclosure) "a circuit combined out of constituent parts," while the accepted meaning ("combinational circuit" being a term on art within the logic circuit art) is "a circuit for which the output value is determined solely by the values of the inputs, such as can be represented by a truth table and computes a Boolean function." The term is indefinite because the specification does not clearly redefine the term.

Correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over JARWALA ET AL. (5,673,276) in view of KOMOIKE (6,094,736).

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Jarwala et al. disclose a semiconductor device comprising a semiconductor wiring substrate 10, said semiconductor wiring substrate 10 being composed of a ceramic, having a wiring ("leads," not shown for the sake of clarity, note column 3 line 53) layer; a plurality of chip IPs 14 mounted on said semiconductor wiring substrate 10 by being bonded thereto; a boundary scan test circuit 16 provided in each of said chip IPs 14; an internal combinational (the amended term "combinatorial" meaning, consistent with applicant's original disclosure, "combined out of constituent parts") circuit provided in each of said chip IPs 14; and scanning signal input terminals 53' and 53 connected to an internal scan chain (note column 5 lines 62-65), at least one of said scanning signal input terminals 53' and 53 being a terminal 53 specially formed separately from said boundary scan test circuit 16; wherein said internal scan chain is for an internal scan test (such as described at column 4 lines 36-47) provided in each of said chip IPs 14, and the boundary scan test circuit 16 and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an internal scan test simultaneously with each other for testing said combinational ("combined out of constituent parts") circuit, using test data for an internal scan test which is input from outside. Note figures 3-6 and 9-12 of Jarwala et al.

Jarwala et al. do not disclose that said ceramic is semiconductor material. However, Komoike discloses a semiconductor wiring substrate 1 being composed of a semiconductor (note figure 1) on which a plurality of semiconductor chip IPs 2,4 are to be mounted; and a plurality of pieces of wiring 7 formed on the semiconductor substrate

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1 to be used only for testing. Note figure 1 of Komoike. Why should one substitute the semiconductor substrate of Komoike for the ceramic substrate of Jarwala et al.? One having skill in the Multi-chip Module Art would know. A mismatch in the materials used for the substrate and the chips bonded thereon could result in a TCE (thermal coefficient of expansion) mismatch. When the assembly is heated, the substrate and chips could expand at different rates, resulting in potentially damaging stress between the constituent parts. This problem is often discussed in the art, for example at column 1 lines 17-40 of Canestaro et al. 4,728,751. Therefore, it would have been obvious to a person having skill in the art to replace the ceramic material of Jarwala et al.'s substrate with the semiconductor material such as taught by Komoike in order to match the material, and thus the CTE, of the chip IPs to thus avoid possible damage due to thermal stress.

Allowable Subject Matter

5. Claims 14 and 15 are allowed over the art of record.

Response to Arguments

6. Applicant's arguments with respect to claims 11,12,13, and 16 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

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information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'T. L. Dickey', with a stylized flourish at the end.

Thomas L. Dickey
Primary Patent Examiner
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